Title: METHOD AND SYSTEM FOR TESTING DRIVER CIRCUITS OF AMOLED

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Cross-Reference to Related Application

[0001] This Application claims priority to Taiwan Patent Application No. 091124960 filed on October 25, 2002.

Field of Invention

[0002] The present invention provides a method and a system for testing circuits of an active matrix organic light emitting display (AMOLED) prior to implantation of organic light emitting diodes (OLEDs).

Background of the Invention

[0003] As technology progresses, the manufacturing technique of monitor display is also progressing. After the technique of liquid crystal display (LCD), the newest technique of monitor display brought to the market is one that utilizes organic light emitting diodes (OLEDs). Each OLED requires a circuit to drive it to emit light. The light can be of either a single color, such as red, green or blue, or even multiple colors. The advantages of OLEDs are the flexibility, liberation from vision angle restriction, long product lifetime and low power consumption.

[0004] Each pixel of an active matrix OLED needs an OLED and a circuit. Therefore, there are ten thousands or even millions of circuits in one panel. It is a complicated task to test the normal functionality of all circuits in one panel. Fig. 1, Fig. 2 and Fig. 3 show the common circuits configured to drive OLEDs within monitor displays. Referring now to Fig. 1, Fig. 2 and Fig. 3, the method of prior art for testing these circuits is to enable each one via the write

scan line WSL and to input a certain voltage level via the data line DL after OLEDs are implanted. The circuit transfers the voltage level into a current signal I which makes the OLED emit light. According to the voltage level, test engineers determine the OLED's functionality simply by observing its luminosity with eyes. Moreover, if a circuit fails the test, the OLED having been implanted in it is wasted and cannot be recovered even though the OLED itself may be perfect. Accordingly, this test method of prior art would result in not only imprecision caused by the subjective decision of the test engineers but also high costs.

Summary of the Invention

[0005] The present invention provides a method and a system to test the circuits within an AMOLED prior to implantation of OLEDs. The AMOLED includes an input panel, a write scan line and a data line.

[0006] The method of the present invention includes the following steps: assigning a value of a data signal to the write scan line, assigning a value of a selection signal to the data line to select a circuit for test, and extracting a signal from a test output terminal of the circuit.

[0007] The system of the present invention includes a data input device, a pixel selection device, and a signal extractor. The data input device is configured to input a data signal. The pixel selection device is configured to input a selection signal to select a circuit. The signal extractor, connected to the test output terminal of the circuit, is configured to extract the current signal.

Brief Description of the Drawings

[0008] Fig. 1 illustrates the first circuitry after implantation of an OLED;

[0009] Fig. 2 illustrates the second circuitry after implantation of an OLED;

[0010] Fig. 3 illustrates the third circuitry after implantation of an OLED;

[0011] Fig. 4 illustrates the first circuitry before implantation of an OLED;

[0012] Fig. 5 illustrates the flow chart of the method provided by the present invention;

[0013] Fig. 6 illustrates the second circuitry before implantation of an OLED;

[0014] Fig. 7 illustrates the third circuitry before implantation of an OLED;

[0015] Fig. 8 illustrates the first exemplary embodiment of the system provided by the present invention; and

[0016] Fig. 9 illustrates the second exemplary embodiment of the system provided by the present invention.

Detailed Description

[0017] The present invention provides a method for testing the circuits within an AMOLED prior to implantation of OLEDs. The AMOLED has a plurality of circuits used to drive a plurality of OLEDs. The AMOLED further includes an input panel, a write scan line and a data line. The input pad is configured to input a selection signal for selecting a circuit and to input a data signal to make the OLED luminous after the OLED has been implanted into the circuit. The write scan line which receives the selection signal from the input panel is configured to enable or disable the circuit. The data line which receives the data signal from the input panel is configured to transmit the data signal to the circuit. Fig. 4 shows one of the common circuits prior to implantation of an OLED. With reference to Fig. 4, a circuit includes a first transistor M41 and a second transistor M43. The first transistor M41 and the second transistor M43 respectively include a source S, a gate G and a drain D. The source S, or the drain, of the first transistor M41 is connected to the data line DL of the AMOLED. The gate G of the first transistor M41 is connected to the write scan line WSL of the

AMOLED. The drain D, or the source, of the second transistor M43 is a test output terminal which will be connected to an OLED after the OLED is implanted.

[0018] Fig. 5 shows the steps of the method provided by the present invention. In step 501, whether all circuits within the AMOLED have been tested is being checked. If the test is not complete, step 503 is executed, in which a value of the data signal is assigned to the data line DL via the input pad. In step 505, a value of the selection signal is assigned to the write scan line WSL via the input pad in order to select a circuit for test. For example, because the first transistor M41 of the circuit in Fig. 4 is a p-channel TFT, the write scan line WSL needs to transmit a low voltage level, in step 505, to the gate G of the first transistor M41 to turn on the first transistor M41. Once the first transistor M41 has been turned on, the data signal assigned in step 503 can enter the circuit. In step 507, a current signal is extracted from the test output terminal, i.e. the drain D, or the source, of the second transistor M43 shown in Fig. 4. In step 509, the current signal is analyzed to determine the normal functionality of the circuit. Then step 501 is executed again to check whether all circuits within the AMOLED have been tested. If still not, steps 503, 505, 507 and 509 are repeated. If yes, step 511 is executed to finish the whole test process.

[0019] For the circuit in Fig. 4, if the initial settings of the power supply VDD and the write scan line WSL are respectively 12V and 0V, the first transistor M41 can be turned on, i.e. the circuit is enabled, so that the data signal is able to enter the circuit. The data signal is a voltage value within a range from 7V to 10V. This range is divided into 64 gray scales in order to drive OLEDs to emit light at 64 different luminous levels. If the circuit can operate perfectly, the expected range of the extracted current signal should be from 20μA to 0.002μA. Also, the range between 20μA and 0.002μA, corresponding to the range of the data signal, can be divided into 64 gray scales. In step 503, the data signal is selected from any of the 64 gray scales within the range from 7V to 10V. If the circuit can operate

perfectly, then the level of the current signal extracted in step 507 should fall in the corresponding gray scale.

[0020] Using the method of the present invention, testing the circuits of an AMOLED can be accomplished precisely and efficiently, and can evade diverse test results caused by subjective decisions of test engineers.

[0021] The circuits shown in Fig. 6 and Fig. 7 are also well known. The difference between those and the circuit shown in Fig. 4 is the types of the first transistors. More specifically, the first transistors M61 and M71 in Fig. 6 and Fig. 7 are n-channel TFTs, but the first transistor M41 in Fig. 4 is a p-channel TFT. Accordingly, the data signal in the write scan line WSL to enable the circuits shown in Fig. 6 and Fig. 7 should be assigned a high voltage level. Besides, the AMOLED with the circuits in Fig. 7 further includes an erase scan line ESL configured to eliminate the potential stored in the capacitor C71 before the data signal enters.

[0022] The method of the present invention can effectively test not only the circuits shown in Fig. 4, Fig. 6, and Fig. 7 but also other similar circuits not mentioned herein.

[0023] The present invention also discloses a system configured to execute the above test method. As Fig. 8 shows, the system includes a data input device 21, a pixel selection device 23, a signal extractor 25 and a signal analyzer 27. The data input device 21 for inputting a value of the data signal 15 is connected to an input pad 13 via a connector 31. The pixel selection device 23 for inputting a value of the selection signal 17 is also connected to the input pad 13 via the connector 31 in order to select a circuit 11. The signal extractor 25 is connected to the test output terminal of the circuit 11 and is configured to extract a current signal 19 from the circuit 11. The signal analyzer 27, connected to the signal extractor 25, is configured to analyze the current signal 19 to determine the normal functionality of the circuit 11.

[0024] With reference to Fig. 8, the signal extractor 25 includes a single test pin. To test the circuit 11, the signal extractor 25 needs moving onto the test output terminal of the circuit 11. Fig. 9 illustrates another exemplary embodiment of the system provided by the present invention. The signal extractor 25 shown in Fig. 9 is capable of testing a row of circuits 11 at one time with its plural test pins. In addition, the signal extractor 25 can also be designed as a test pin array with which all circuits can be tested without the signal extractor 25 being moved.

[0025] The above description of the preferred embodiments is expected to clearly expound the characteristics of the present invention but not expected to restrict the scope of the present invention. Those skilled in the art will readily observe that numerous modifications and alterations of the apparatus may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the bounds of the claims.